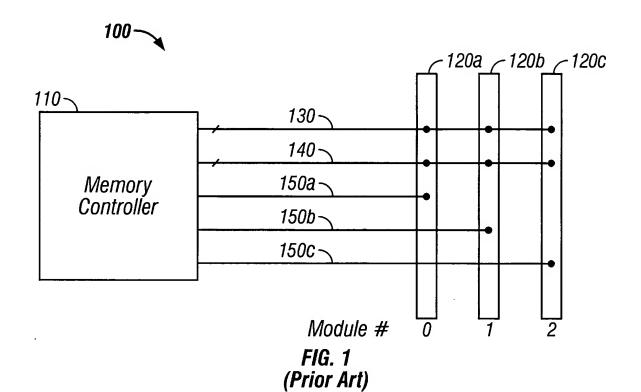
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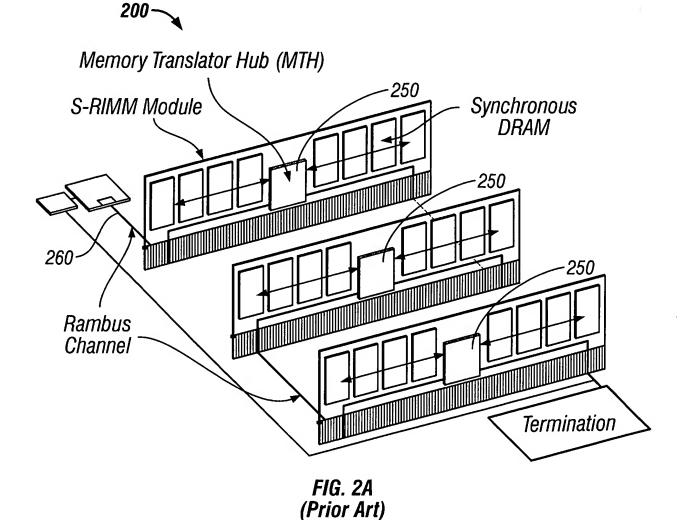
Title: CONFIGURABLE WIDTH BUFFERED MODULE

Applicants: Richard Perego et al.
Appl. No.: Unknown
Filing Date: Herewith

Docket: RAMB-01049US2 Atty: Kirk J. DeNiro, Esq. Phone: (415) 369-9660

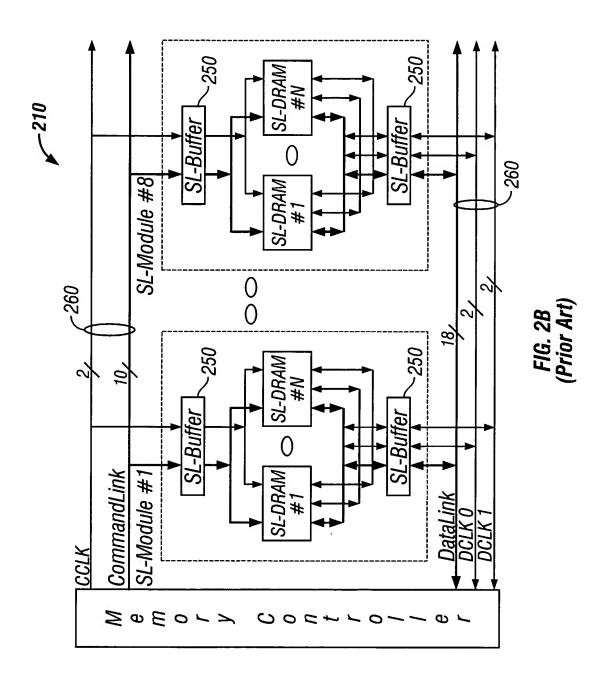
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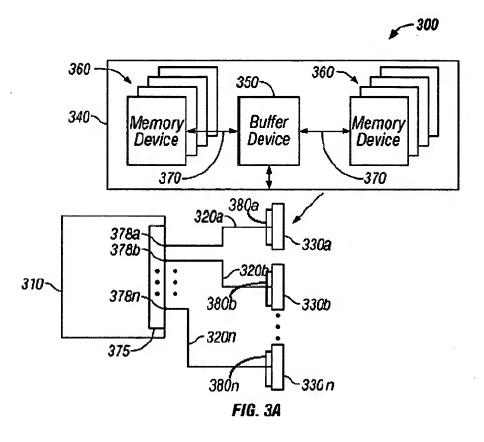
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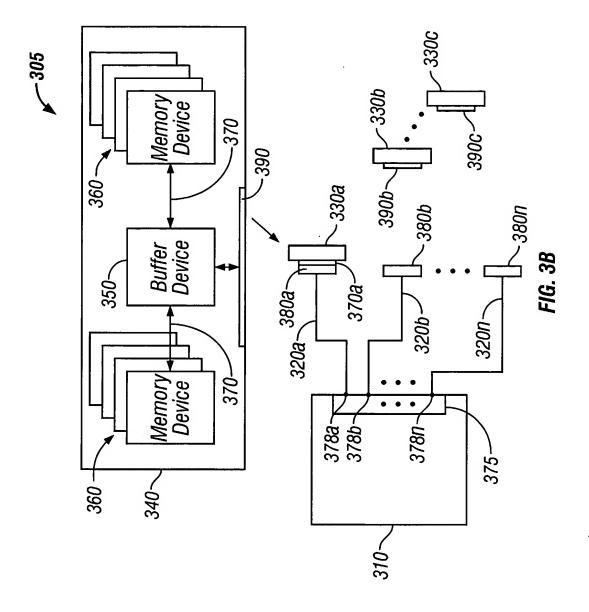
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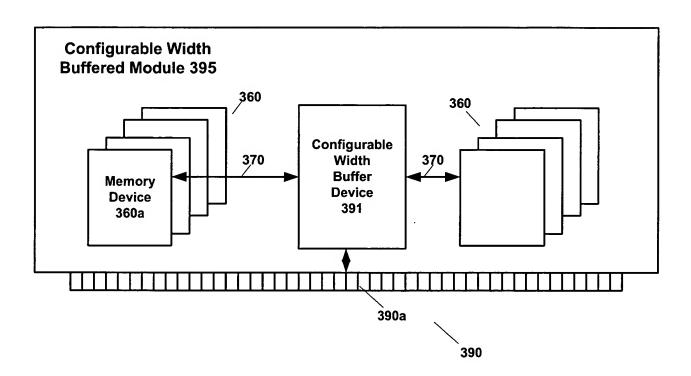
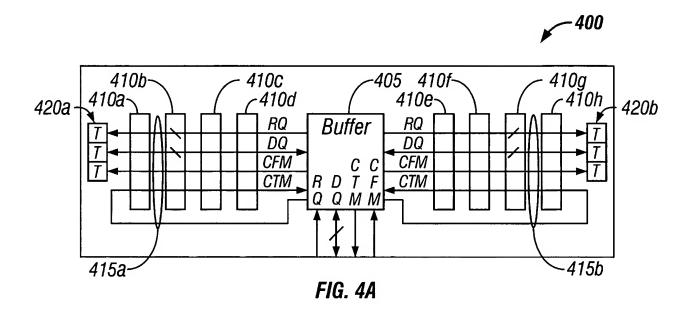


Fig. 3C

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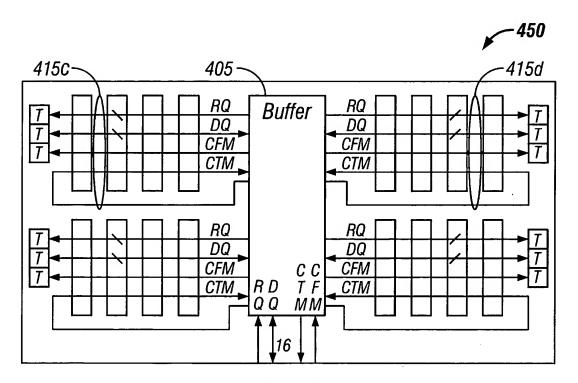


FIG. 4B

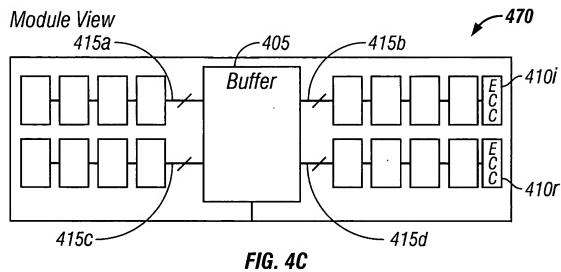
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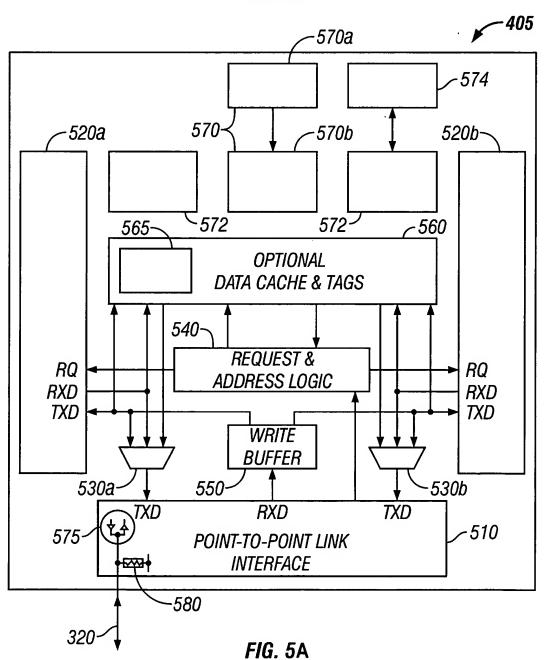
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Configurable 570a 574 Width Buffer Device 391 572 570b 572 W<sub>RQ,S</sub> W<sub>RQ,S</sub> **OPTIONAL** 565 **DATA CACHE & TAGS** 560 WDPTS W<sub>DPT,S</sub> 520a 520b **REQUEST &**  $\mathbf{W}_{\mathtt{DPTS}}$ W<sub>DPT,S</sub> **→**RQ RQ **ADDRESS LOGIC** 540 **RXD RXD** WDPTS W<sub>DPT,S</sub> **TXD TXD** WDPTS  $\mathbf{W}_{\mathsf{DPT,S}}$ 576 **595** 530a 530b **Configurable Serialization 591 ₹W**<sub>DP</sub> Interface 596 575 580 <u>₩₩</u> **Configurable Width Interface 590**  $W_{DP} = 1, 2, 4, 8, 16, 32,$ 64,128 Fig. 5B

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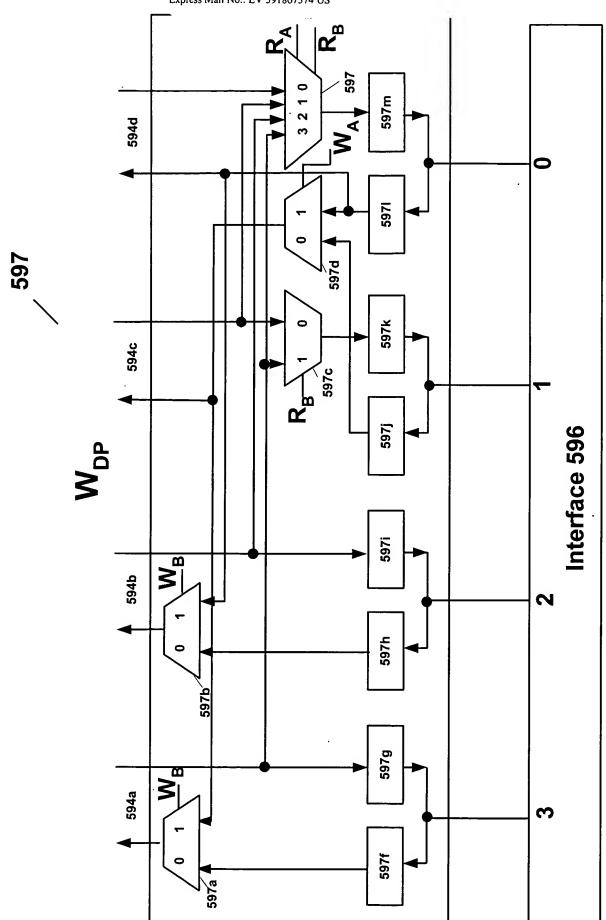


Fig. 5C

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Width	Write		Read		Interface 596
	W <sub>A</sub>	W <sub>B</sub>	R <sub>A</sub>	R <sub>B</sub>	Connections
1	1	1	A <sub>0</sub>	A <sub>1</sub>	0
2	0	1	0	A <sub>0</sub>	0 and 1
4	0	0	0	0	3, 2, 1 and 0

Fig. 5D

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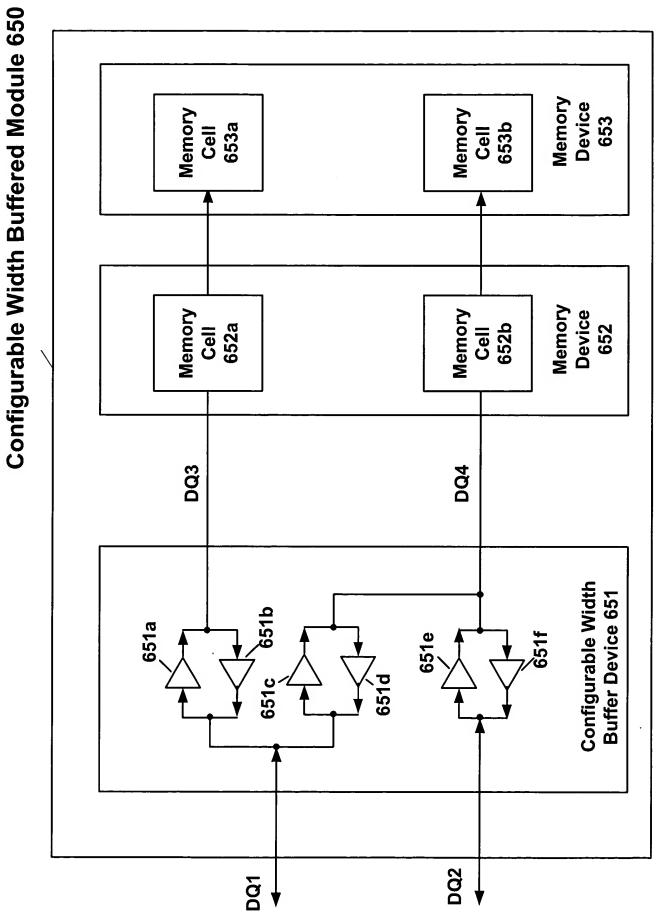
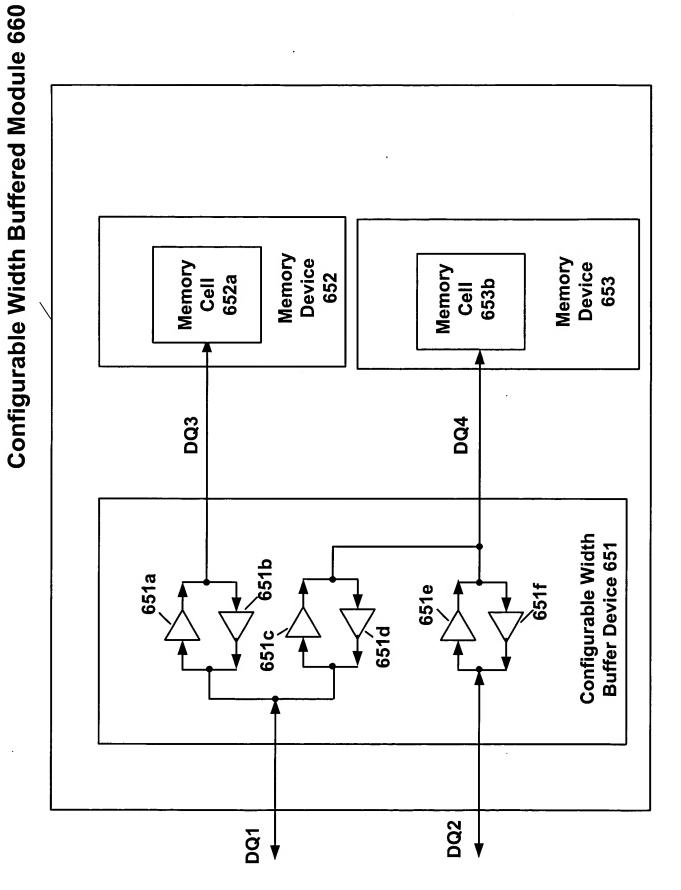


Fig. 5E

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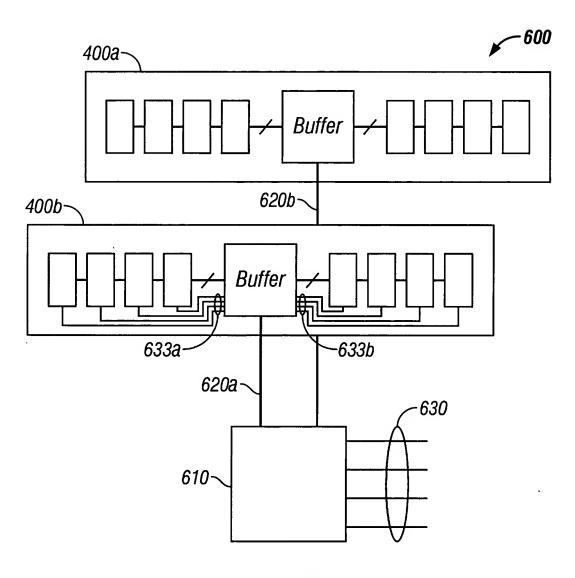


FIG. 6A

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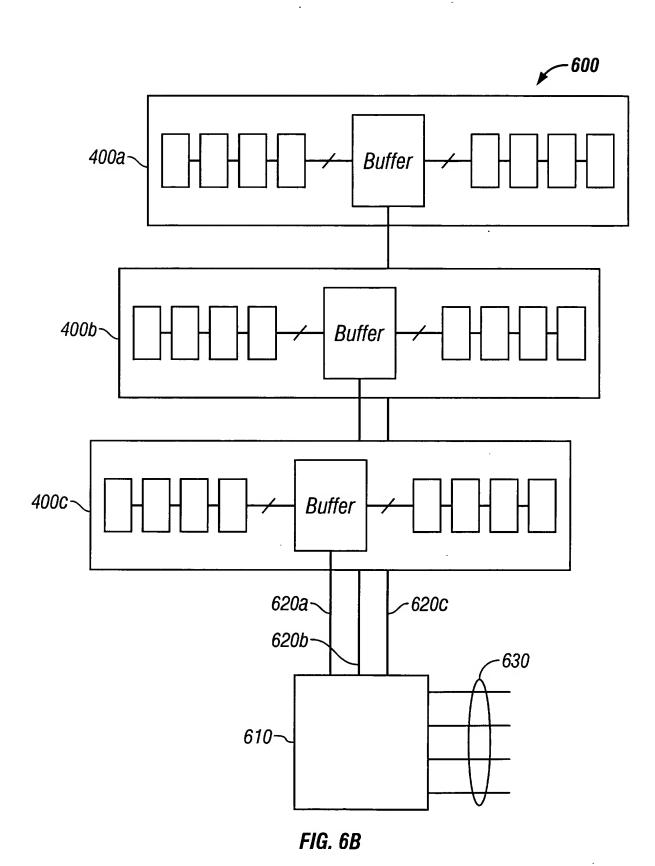
Title: CONFIGURABLE WIDTH BUFFERED MODULE
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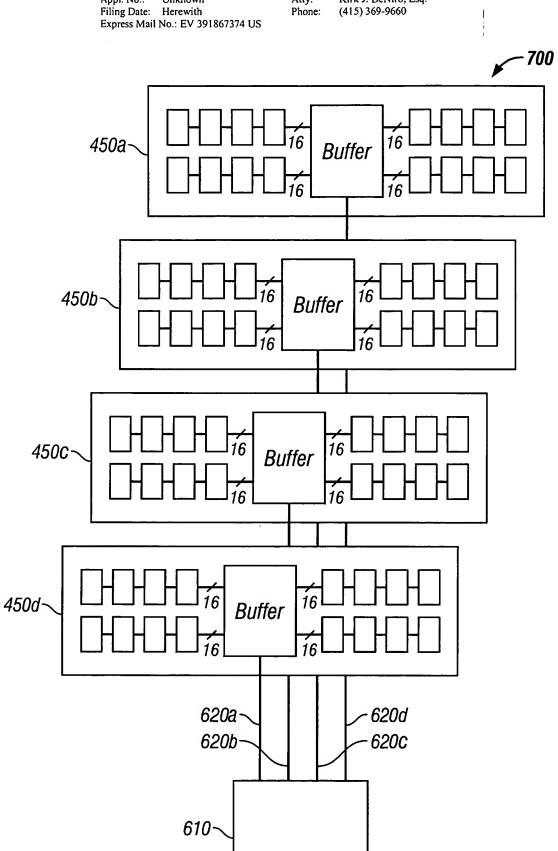


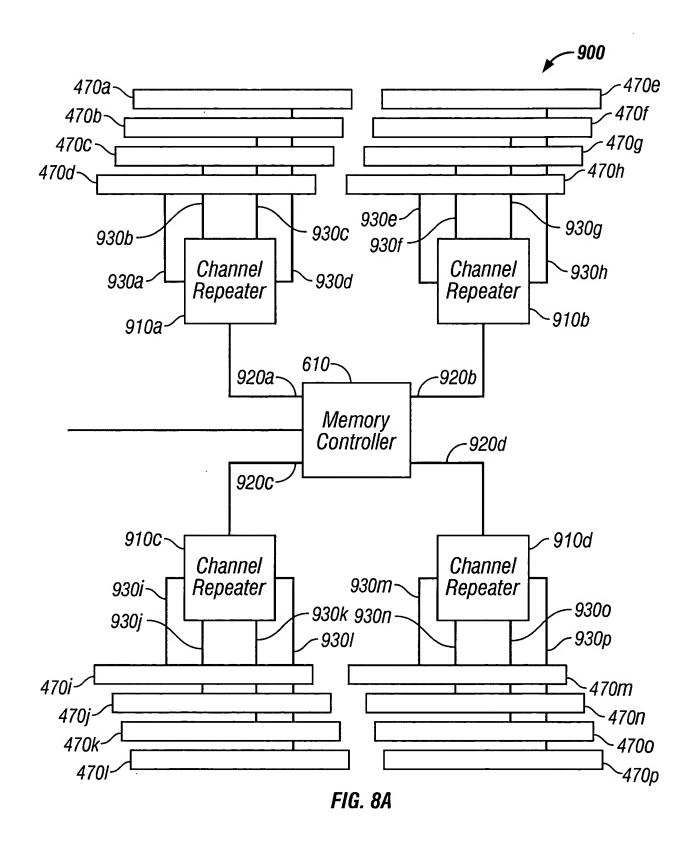
FIG. 7

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960b 960c -960d 960a-950c-950a-950b-950d-

FIG. 8B

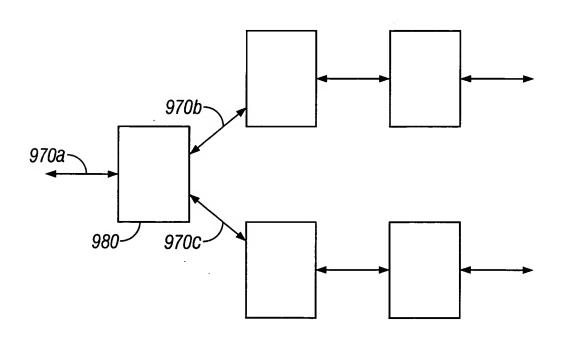


FIG. 8C